ECE 510/511 and EE 410/411 Syllabus

Computer Design and Lab

Dr. John Naber

General Information

- Dr. John Naber: john.naber@louisville.edu
- Office: Belknap Research Bldg #238
- Office Hours: 9:00 to 5:30 Mon thru Fri
- Text Book: Circuit Design with VHDL by Volnei Pedroni, 2nd Edition, MIT Press, 2010 (< $50 new)
- Notes emailed directly to WKU students and will use DELO for taking 2 tests
- Will use Xilinx Vivado software for the labs and hardware project
- WKU Disability Statement: “In compliance with university policy, students with disabilities who require academic and/or auxiliary accommodations for this course must contact the Office for Student Disability Services in Downing University Center, A-200. The phone number is (270) 745-5004. Please DO NOT request accommodations directly from the professor or instructor without a letter of accommodation from the Office for Student Disability Services.

Revised 2015 Title IX/Clery Syllabi Statement (6.9.2015)

The following statement should be added to all course syllabi, beginning July 1, 2015.

Title IX/Clery Act Notification

Sexual misconduct (including sexual harassment, sexual assault, and any other nonconsensual behavior of a sexual nature) and sex discrimination violate University policies. Students experiencing such behavior may obtain **confidential** support from the PEACC Program (852-2663), Counseling Center (852-6585), and Campus Health Services (852-6479). To report sexual misconduct or sex discrimination, contact the Dean of Students (852-5787) or University of Louisville Police (852-6111).

Disclosure to **University faculty or instructors** of sexual misconduct, domestic violence, dating violence, or sex discrimination occurring on campus, in a University-sponsored program, or involving a campus visitor or University student or employee (whether current or former) is **not confidential** under Title IX. Faculty and instructors must forward such reports, including names and circumstances, to the University's Title IX officer.

For more information, see the Sexual Misconduct Resource Guide (http://louisville.edu/hr/employeerelations/sexual-misconduct-brochure).

ECE 510: Computer Design

Text: "*Circuit Design with VHDL*" by Pedroni

DATE	Class #	TOPICS
8-28-18	1	Section I: Importance of digital IC design, product & job examples, product teardown
8-30-18	2	IC Design flow, IC parasitics, ASIC Methodologies
9-4-18	3	ASIC Methodologies
9-6-18	4	Digital IC Test Methods
9-11-18	5	Digital IC Test Methods, Importance of Yield, 6σ quality
9-13-18	6	IC Packaging and Time to Market Importance
9-18-18	7	Moore's Law
9-20-18	8	Encoders and Decoders, Gate and Flip-Flop Timing Parameters
9-25-18	9	Noise Margin, DFFs, TFFs, Latches, Multiplexers
9-27-18	10	Finding fmax in DFF stages, Low power digital design
10-2-18	11	Section II: Introduce Xilinx Vivado, FPGA Design, post labs, review for test
10-4-18	12	Test #1 and Research Paper Due*
10-9-18		No class, UofL Fall Break
10-11-18		No class, WKU Fall Break
10-16-18	13	FPGA Design, Lab #1 due
10-18-18	14	VHDL Introduction, Chapter 1, Chapter 2: Code Structure, last day to withdraw
10-23-18	15	Chapter 3: Data Types, Lab #2 due
10-25-18	16	Chapter 3: Data Types, Lab #3 due
10-30-18	17	Chapter 4: Operators and Attributes, Review Hardware Project & Select Teams
11-1-18	18	Chapter 4: Operators and Attributes, Lab#4 due
11-6-18	19	Section III: Chapter 5: Concurrent Code, Lab #5 due
11-8-18	20	Chapter 5: Concurrent Code, Lab #6 due
11-13-18	21	Chapter 6: Sequential Code Lab #7 due
11-15-18	22	Chapter 6: Sequential Code, , Lab #8 due
11-20-18	23	Test #2
11-22-18		No class, Thanksgiving break
11-27-18	24	Chapter 7: Signals and Variables, Lab#9 due Sequential Code
11-29-18	25	Chapter 8: Hierarchical design using packages & components, Lab #10 due, last class
12-10-18		Optional Final: 3 to 5:30 EST in SRB, Hardware Project Due

*** Research Paper required only for UofL students taking ECE 510 for graduate credit**

- **2100 minutes required per course. Need to make up 3 missed classes (8-22, 8-24 & 10-11).**
- **2100 minutes / 25 classes = 84 minutes per class (9 minutes additional per class)**
- **Therefore, each class will go from 4:00 to 5:24 EST**

ABET Course Learning Outcomes

Course Learning Outcome (CLO)	Activity	Related PO
Students who complete this course will be able to:		
1. Understand the tasks of digital designers and be able to make design-based decisions between the 4 digital custom ASIC methodologies: full custom, standard cell, gate array and programmable logic.	Hmwks: 1,2,3,4	5
2. Describe general test and packaging methods for digital engineers and the importance of yield on cost & test.	Hmwks: 5,6	5
3. Describe the importance of time to market and Moore's Law for digital engineers. Describe various methods used to reduce power consumption in digital ICs.	Hmwks: 1,7,8,9	5
4. Understand the function and timing diagrams for a variety of basic digital circuits such as: DFF's, TFF's, latches, multiplexers, comparators, encoders, decoders, counters, parity generators & detectors, shift registers, barrel shifters, adders and ALUs.	Hmwks:10,12,	3
5. Use VHDL to create the digital circuits listed in (4) above as well as other custom digital designs with correct syntax.	Hmwks: 14,15 Labs: 1 to 10 Hardware project	3
6. Use computer-based tools, such as Xilinx Vivado to design digital circuits in VHDL, similar to those listed in (3) above.	Labs: 1 to 10	3, 11
7. Describe the advantages of using FPGAs in product design. Be able to translate the FPGA's Configurable Logic Gates (CLBs) into equivalent logic gates.	Hmwks: 13 Hardware project	5
8. Demonstrate effective teamwork skills and written communication from the hardware project and research paper	Research Paper Hardware project	4, 7b

Grading

ECE 510:

- Two Tests = 50% (Final optional, can replace a test grade)
- Homework = 35%, 15 homeworks (late homework not accepted)
- One hardware / software project = 10% (2-person teams)
- Research paper (for graduate credit) = 5%: 5-page typed (2X space, 12 pt. font) report, describing a paper on digital design topic. Must have at least one IEEE reference (see IEEE.org website, IEEE Xplore on top right of web page to search for articles). * Due day of first test.
  - M.S., M.Eng., Ph.D. and undergraduate students taking 510 for graduate credit must complete the research paper.
  - Undergraduates (UofL and WKU) not taking 510 for graduate credit must notify instructor and their 510 grade will be scaled to not include the paper.

ECE 511: (make sure you register for the course and the lab)

- **10 software labs using VHDL = 100% (some will require using dev board)**
  - **Each person must submit their own lab report, but you are allowed to work in groups.**
  - **Open lab: you do on your own time and PC (or school PC).**
  - **Late labs not accepted if you don't email instructor before due date.**

Letter Grades

A+ = 97 to 100	C+ = 77 to 79	F < 60
A = 93 to 96	C = 73 to 76	
A- = 90 to 92	C- = 70 to 72	
B+ = 87 to 89	D+ = 67 to 69	
B = 83 to 86	D = 63 to 66	
B- = 80 to 82	D- = 60 to 62	

Academic Dishonesty & Plagiarism:

Any cases can result in disciplinary action including an 'F' for the course and suspension or expulsion from the university